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10/632,241	08/01/2003	Soo Keong Ong	42P16798	3317

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EXAMINER	
PATEL, NIKETA I	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/632,241	ONG ET AL.	
	Examiner	Art Unit	
	Niketa I. Patel	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4-6, 8-11, 13-14, 16-17, 19-21, 23-26, 28-29 and 35-36 rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. U.S. 6,421,798 B1 (hereinafter '*Lin*'.)

3. **Referring to claims 1, 9, 16, 24**, *Lin* teaches, in taking claim 1 as exemplary, a circuit comprising: a first device [see figure 3, element 104, system BIOS] coupled with a first bus [see figure 3, element 330, ISA bus], wherein the first device is not compliant with a standard [see column 4, lines 52-59, System BIOS 104 is ISA compliant], the first device containing data, wherein the data is not operational for the circuit with a device that is not compliant with the standard [see column 3, lines 50-55, BIOS code]; a second device [see figure 3, element 114] coupled with a second bus [see figure 3, element 308, PCI bus], wherein the second device is compliant with the standard [see column 4, lines 52-59, Test card 114 is compliant with PCI], the second device to be associated with the data from the first device, the association of the second device with the data from the first device enabling the data to be utilized according to the standard [see column 7, lines 4-10, BIOS codes is transferred to the test card memory 320 from the system BIOS 104; *Note*: *the limitation of 'to be associated with' does not provide structural limitation to how the data is associated with the second device*]; and a memory [see figure 3, element 106] to receive the data from the first device [see column 6, lines 24-30, BIOS code is

loaded into cache 106 from system BIOS 104 by first writing it into memory locations associated with PCI address space.]

4. **Referring to claim 2**, *Lin* teaches further comprising a plurality of devices [see figure 3, element 318 and column 4, lines 33-38, several PCI slots for accommodating PCI-compatible adapter cards] coupled with the second bus [see figure 3, element 308, PCI bus], wherein each of the plurality of devices is compliant with the standard [see column 4, lines 33-38, several PCI slots for accommodating PCI-compatible adapter cards], and wherein the plurality of devices includes the second device [see column 4, lines 33-38, PCI test card 114 inserted into one of the PCI slots 318.]

5. **Referring to claim 4**, *Lin* teaches wherein the second device comprises a function of a physical device [see figure 3, element 114, test card with memory, CPU and plurality of interfaces.]

6. **Referring to claim 5**, *Lin* teaches wherein the first device comprises flash memory [see column 4, lines 66-67 and column 5, lines 1, 'the BIOS flash ROM 104'.]

7. **Referring to claim 6**, *Lin* teaches wherein the data comprises an operating [see column 3, lines 14-20, BIOS code which provides boot instructions/ star-up code for computer's basic input/output system.]

8. **Referring to claim 8**,*Lin* teaches wherein the standard comprises a PCI (peripheral component interconnect) specification [see column 4, lines 33-35, PCI], and wherein the second bus is a PCI bus [see figure 3, element 308, PCI bus.]

9. **Referring to claim 10**, *Lin* teaches wherein identifying the standard peripheral device comprises choosing the standard peripheral device from a plurality of standard peripheral devices

[see figure 3, elements 318, 114] that are coupled with the first bus [see figure 3, element 308 and column 4, lines 33-38, test card 114 is chosen to be used over the other PCI slots 318.]

10. **Referring to claim 11**, *Lin* teaches wherein choosing the standard peripheral device comprises pre-selecting the standard peripheral device before commencing operations [see column 4, lines 33-38, test card 114 is pre-selected before sending the data to the test card.]

11. **Referring to claim 13**, *Lin* teaches wherein the standard comprises a PCI (peripheral component interconnect) specification [see column 4, lines 33-35, PCI.]

12. **Referring to claim 14**, *Lin* teaches wherein the data comprises an operating system [see column 3, lines 14-20, boot instructions, interface for to the underlying hardware for the operating system in the form of a library of interrupt handlers.]

13. **Referring to claim 17**, *Lin* teaches wherein the computer system is an embedded system [see column 3, lines 41-48, i.e. a special purpose (embedded) computer system.]

14. **Referring to claim 19**, *Lin* teaches wherein the plurality of devices includes one or more function of a physical deivce [see figure 3, element 114, test card with memory, CPU and plurality of interfaces.]

15. **Referring to claim 20**, *Lin* teaches wherein the first device comprises flash memory [see column 4, lines 66-67 and column 5, lines 1, 'the BIOS flash ROM 104'.]

16. **Referring to claim 21**, *Lin* teaches wherein the data comprises an operating system [see column 3, lines 14-20, BIOS code which provides boot instructions/ star-up code for computer's basic input/output system.]

17. **Referring to claim 23**, *Lin* teaches wherein the standard comprises a PCI (peripheral component interconnect) specification [see column 4, lines 33-35, PCI.]

18. **Referring to claim 25**, *Lin* teaches wherein identifying the standard peripheral device comprises choosing the standard peripheral device from a plurality of standard peripheral devices [see figure 3, elements 318, 114] that are coupled with the first bus [see figure 3, element 308 and column 4, lines 33-38, test card 114 is chosen to be used over the other PCI slots 318.]

19. **Referring to claim 26**, *Lin* teaches wherein choosing the standard peripheral device comprises pre-selecting the standard peripheral device before commencing operations [see column 4, lines 33-38, test card 114 is pre-selected before sending the data to the test card.]

20. **Referring to claim 28**, *Lin* teaches wherein the standard comprises a PCI (peripheral component interconnect) specification [see column 4, lines 33-35, PCI.]

21. **Referring to claim 29**, *Lin* teaches wherein the data comprises an operating system [see column 3, lines 14-20, BIOS code which provides boot instructions/ star-up code for computer's basic input/output system.]

22. **Referring to claim 35**, *Lin* teaches wherein the choice of the standard peripheral devices from the plurality of standard peripheral devices is performed by a first controller [see figure 3, element 328] that is coupled with the first bus and the second bus [see figure 3, elements 308, 330 and column 4, lines 52-63, the PCI-to-ISA bridge provides interface from the PIC bus to the ISA bus.]

23. **Referring to claim 36**, *Lin* teaches wherein the dispatching of the data to memory [see figure 3, element 106] comprises transferring the data to memory via a second controller [see figure 3, element 304] that is coupled with the memory and the first controller [see figure 3, element 328 and column 6, lines 24-30, column 7, lines 4-10, column 1, lines 26-29, BIOS code is loaded from 104 to 106 by using the PCI address space of 320.]

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

26. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Lin* in view of Powderly et al. U.S. Patent Number: 6,560,641 (hereinafter "*Powderly*".)

27. **Referring to claim 22**, *Lin* teaches wherein the data includes a boot loader [see column 3, lines 14-20, 'booting instructions'] however does not teach the boot loader being stored as an option-ROM for the first device. *Powderly* teaches this limitation [see *Powderly* column 4, lines 37-41] in order to provide additional BIOS level control of certain low-level features.

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the system of *Lin* to be able to include BIOS

extensions (Option ROM) in order to provide additional BIOS level control of certain low-level features. It is for this reason that one of ordinary skill in the art would have been motivated to implement system of *Lin* with Option-ROM.

28. Claims 3, 12, 18, 27 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Lin* in view of Ma U.S. Patent App. Pub. Number: 2004/0003297 A1 (hereinafter "*Ma*".)

29. **Referring to claims 3, 18, 32**, *Lin* teaches further comprising a controller coupled with the first bus and the second bus [see figure 3, element 328] however does not set forth the limitation of scanning the plurality of standard devices to identify the second device [see figure, element]. *Ma* teaches to scan the plurality of standard devices to identify the second device [see *Ma* paragraph 0032-0033, 'enumeration', 'configuration', 'scan the PCI bus'] in order to determine which types of devices are present and enabling these devices for communication.

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the system of *Lin* to be able to determine the types of devices that are present and enabling the present device for communication. It is for this reason that one of ordinary skill in the art would have been motivated to implement system of *Lin* to be able to determine device types and enabling the device for communication.

30. **Referring to claims 12, 27**, *Lin* teaches further comprising a controller coupled with the first bus and the second bus [see figure 3, element 328] however does not set forth the limitation of wherein choosing the standard peripheral device comprises scanning the plurality of standard peripheral devices coupled with the first bus to identify a suitable device. *Ma* teaches to scan the plurality of standard devices to identify the second device [see *Ma* paragraph 0032-0033,

'enumeration', 'configuration', 'scan the PCI bus'] in order to determine which types of devices are present and enabling these devices for communication.

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the system of *Lin* to be able to determine the types of devices that are present and enabling the present device for communication. It is for this reason that one of ordinary skill in the art would have been motivated to implement system of *Lin* to be able to determine device types and enabling the device for communication.

31. **Referring to claims 31, 34**, *Lin* teaches further comprising a second controller [see figure 3, element 304] coupled with the controller [see figure 3, element 328] and the memory [see figure 3, element 106], wherein the memory receives the data via the second controller [see column 6, lines 24-30, column 7, lines 4-10, column 1, lines 26-29, BIOS code is loaded from 104 to 106 by using the PCI address space of 320.]

32. **Referring to claim 33**, *Lin* teaches wherein the dispatching of the data to memory [see figure 3, element 106] comprises transferring the data to memory via a second controller [see figure 3, element 304] that is coupled with the memory and the first controller [see figure 3, element 328 and column 6, lines 24-30, column 7, lines 4-10, column 1, lines 26-29, BIOS code is loaded from 104 to 106 by using the PCI address space of 320.]

33. Claims 7, 15 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Lin* in view of *Ma* and Powderly et al. U.S. Patent Number: 6,560,641 (hereinafter "*Powderly*".)

34. **Referring to claims 7, 15, 30**, *Lin* teaches wherein the data includes a boot loader [see column 3, lines 14-20, 'booting instructions'] however does not teach the boot loader being

stored as an option-ROM for the first device. *Powderly* teaches this limitation [see *Powderly* column 4, lines 37-41] in order to provide additional BIOS level control of certain low-level features. One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the system of *Lin* to be able to include BIOS extensions (Option ROM) in order to provide additional BIOS level control of certain low-level features. It is for this reason that one of ordinary skill in the art would have been motivated to implement system of *Lin* with Option-ROM.

Response to Arguments

35. Applicant's arguments filed 01/10/2007 have been fully considered but they are not persuasive. The applicant argues that the operation of *Lin* does not provide any teaching or suggestion of data that is not operational with a deivce that is not compliant with a standard being associated with a second device that is compliant with the standard, with the association of the second device with the data from the first device enabling the data to be utilized according to the standard (see pages 10-12 of the remarks.)

The examiner respectfully disagrees with this argument. *Lin* clearly discloses a first device [figure 3, element 104 – system BIOS] coupled with a first bus [figure 3, element 330 – ISA bus] and a second device [figure 3, element 114] coupled with a second bus [figure 3, element 308 – PCI bus], wherein the first device is not compliant with a standard [system BIOS is ISA compliant] and the second device is compliant with the standard [test card 114 is PCI compliant] and associating the second deivce with the data from the first device so that the data can be utilized according to the standard [column 6, lines 24-34 – to enable caching of the

portion of high-speed BIOS code (i.e., 'the data'), a loader routine in the enhanced BIOS code causes the high-speed code to be loaded into cache memory by first writing it into memory locations associated with a high-speed address space of PCI address space- meaning the code from the BIOS is associated with the PCI protocol in order allow the PCI device to utilize the code/data.]

Conclusion

36. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (571) 272 4156. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272 4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Niketa Patel
05/03/2007

DONALD SPARKS
SUPERVISORY PATENT EXAMINER